

### **Amendments to the Claims**

Claim 1 (**Currently Amended**) A semiconductor ~~device, device~~ comprising:  
a substrate including an integrated circuit;  
an interlayer insulating layer formed on said substrate, said interlayer insulating layer having a contact hole;  
a ferroelectric capacitor formed by a first electrode layer, a ferroelectric layer and a second electrode layer deposited on said interlayer insulating layer in this order;  
a wiring layer electrically connecting said second electrode layer of said ferroelectric capacitor to said integrated circuit through ~~a~~ said contact hole in said interlayer insulating layer; and  
an insulating side wall film covering a peripheral section of said ferroelectric capacitor electrically insulating said peripheral section of said ferroelectric capacitor from said wiring layer, and being spaced from a peripheral edge section of said contact hole.

Claim 2 (**Currently Amended**) The semiconductor device according to the claim 1, wherein said ~~integrated circuit~~ wiring layer includes a contact plug within said contact hole ~~and said wiring layer electrically connects to said contact plug~~.

Claim 3 (**Currently Amended**) The semiconductor device according to the claim 2, wherein said interlayer insulating layer includes a plug oxidation protective film ~~consisting of~~ comprising silicon nitride ~~and silicon oxide~~, and said ferroelectric capacitor is mounted on said interlayer insulating layer.

Claim 4 (**Previously Presented**) The semiconductor device according to the claim 1, wherein said insulating side wall film includes a hydrogen diffusion preventing layer.

Claim 5 (**Currently Amended**) The semiconductor device according to the claim 1, wherein said ferroelectric layer ~~consists of~~ comprises bismuth strontium tantalate.

Claims 6-11 (**Cancelled**)

Claim 12 (**New**) The semiconductor device according to claim 1, wherein at least a portion of said wiring layer is deposited on said insulating side wall film.

Claim 13 (**New**) The semiconductor device according to claim 1, wherein an upper surface of said second electrode layer is free of said insulating side wall film.